IN THE CLAIMS

Please amend claim 1. Please add new claims 30-34. All currently pending claims and status indicators are set forth below. This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A method of processing a request in a computer system, comprising the acts of:

(a) initiating a read request from a requesting agent, the requesting agent residing on a bus, wherein the read request has an address corresponding to a memory location;

(b) receiving the read request at a processor controller;

(c) sending the read request from the processor controller to an access controller;

(d) sending a deferred reply from the processor controller to the requesting agent when the processor controller is free to process the read request, wherein the deferred reply is sent before data corresponding to the read request is delivered to the access controller;

(e) delivering data residing at the address corresponding to the memory location to the access controller;

(f) delivering the data from the access controller to the processor controller; and

(g) delivering the data from the processor controller to the requesting agent.

2. (Original) The method of processing a request, as set forth in claim 1, comprising the act of sending a data ready signal from the access controller to the processor controller upon receipt of the data at the access controller.

3. (Original) The method of processing a request, as set forth in claim 1, wherein act (a) comprises the act of initiating a read request from a processor residing on a processor bus.

4. (Original) The method of processing a request, as set forth in claim 1, wherein act (a) comprises the act of initiating a read request from a peripheral device residing on an input/output (I/O) bus.

5. (Original) The method of processing a request, as set forth in claim 1, wherein act (c) comprises the act of sending the request from the processor controller to a memory controller.

6. (Original) The method of processing a request, as set forth in claim 1, wherein act (c) comprises the act of sending the request from the processor controller to a tag controller.

7. (Original) The method of processing a request, as set forth in claim 1, wherein act (d) comprises the act of sending a deferred reply immediately upon the agent bus being available to receive data from the memory location.

8. (Original) The method of processing a request, as set forth in claim 1, wherein act (d) comprises the act of waiting a predetermined number of clock cycles after the deferred reply is sent before delivering data.

9. (Original) The method of processing a request, as set forth in claim 1, wherein acts (d) and (f) are performed simultaneously.

10. (Original) The method of processing a request, as set forth in claim 1, wherein the acts are performed in the recited order.

11. (Original) A method of processing a request in a computer system, comprising the acts of:

(a) sending a request from a processor controller to an access controller on a first clock cycle, the request originating from an agent; and

(b) sending a deferred reply from the processor controller to the agent on a second clock cycle, the second clock cycle being immediately subsequent to the first clock cycle.

12. (Original) The method of processing a request, as recited in claim 11, wherein act (a) comprises the act of sending a request from a processor controller to a memory controller on a first clock cycle.

13. (Original) The method of processing a request, as set forth in claim 11, wherein act (a) comprises the act of sending a request for a processor controller to a tag controller on a first clock cycle.

14 – 18. (Canceled)

19. (Original) A computer system comprising:

a plurality of buses;

a memory system operably coupled to the plurality of buses; and

a processor controller coupled to each of the plurality of buses and configured to simultaneously issue a deferred reply to a requesting device in response to receiving a read request from the requesting device and obtain the data corresponding to the read request from the memory system.

20. (Original) The computer system, as set forth in claim 19, wherein at least one of the plurality of buses comprises a processor bus.

21. (Original) The computer system, as set forth in claim 19, wherein at least one of the plurality of buses comprises an input/output (I/O) bus.

22. (Original) The computer system, as set forth in claim 19, wherein the processor controller is further configured to obtain the data corresponding to the read request from the memory system before issuing a deferred reply to a requesting device.

23. (Original) The computer system, as set forth in claim 19, wherein the memory system comprises a redundant memory system.

24-29. (Canceled)

30. (New) A computer system comprising:

a memory system;

a requesting agent operably coupled to the memory system and configured to initiate read requests to the memory system; and

a processor controller coupled between the memory system and the requesting agent and configured to send a deferred reply from the processor controller to the requesting agent when the processor controller is free to process the read request, regardless of whether data corresponding to the read request has been delivered from the memory system to the processor controller.

31. (New) The computer system, as set forth in claim 30, wherein the requesting agent comprises a processor.

32. (New) The computer system, as set forth in claim 30, wherein the requesting agent comprises an input/output (I/O) device.

33. (New) The computer system, as set forth in claim 30, wherein the processor controller is configured to obtain the data corresponding to the read request from the memory system before issuing a deferred reply to the requesting agent.

34. (New) The computer system, as set forth in claim 30, wherein the memory system comprises a redundant memory system.